

# DATA SHEET

**74ABT16823A**

**74ABTH16823A**

18-bit bus interface D-type flip-flop  
with reset and enable (3-State)

Product specification  
Supersedes data of 1995 Sep 28  
IC23 Data Handbook

1998 Feb 27

# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

**74ABT16823A**  
**74ABTH16823A**

## FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16823A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up Reset
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}$ ; GND = 0V	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nCP to nQx	$C_L = 50\text{pF}$ ; $V_{CC} = 5\text{V}$	2.3 1.9	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	4	pF
$C_{OUT}$	Output capacitance	$V_O = 0\text{V}$ or $V_{CC}$ ; 3-State	6	pF
$I_{CCZ}$	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	$\mu\text{A}$
		Outputs low; $V_{CC} = 5.5\text{V}$	9	mA

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT16823A DL	BT16823A DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT16823A DGG	BT16823A DGG	SOT364-1
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ABTH16823A DL	BH16823A DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABTH16823A DGG	BH16823A DGG	SOT364-1

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}, 2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}, 2\overline{CE}$	Clock enable input (active-Low)
1, 28	1MR, 2MR	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	$V_{CC}$	Positive supply voltage

**18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)**

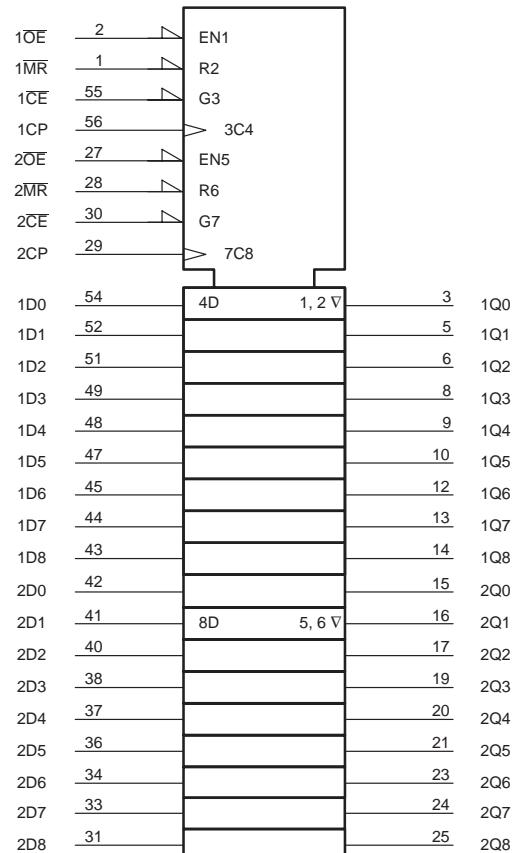
**74ABT16823A  
74ABTH16823A**

**PIN CONFIGURATION**

1 $\overline{MR}$	1	56	1CP
1 $\overline{OE}$	2	55	1CE
1Q0	3	54	1D0
GND	4	53	GND
1Q1	5	52	1D1
1Q2	6	51	1D2
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1Q3	8	49	1D3
1Q4	9	48	1D4
1Q5	10	47	1D5
GND	11	46	GND
1Q6	12	45	1D6
1Q7	13	44	1D7
1Q8	14	43	1D8
2Q0	15	42	2D0
2Q1	16	41	2D1
2Q2	17	40	2D2
GND	18	39	GND
2Q3	19	38	2D3
2Q4	20	37	2D4
2Q5	21	36	2D5
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2Q6	23	34	2D6
2Q7	24	33	2D7
GND	25	32	GND
2Q8	26	31	2D8
2 $\overline{OE}$	27	30	2CE
2 $\overline{MR}$	28	29	2CP

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**LOGIC SYMBOL (IEEE/IEC)**

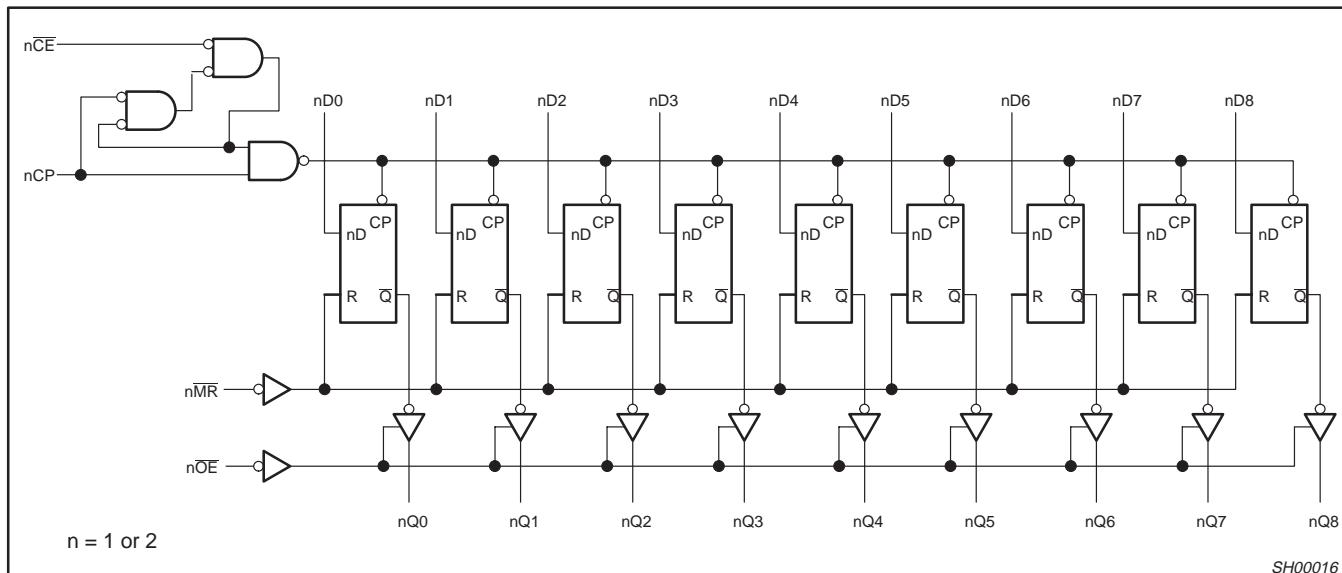


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# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
nOE	nMR	nCE	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	I	L	
L	H	H	↑	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level

I = Low voltage level one set-up time prior to the Low-to-High clock transition

NC = No change

X = Don't care

Z = High impedance "off" state

↑ = Low to High clock transition

‡ = Not a Low-to-High clock transition

# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		−0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	−18	mA
$V_I$	DC input voltage <sup>3</sup>		−1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	−50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	−0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	128	mA
		output in High state	−64	
$T_{stg}$	Storage temperature range		−65 to 150	°C

### NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		−32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_{amb}$	Operating free-air temperature range	−40	+85	°C

# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT	
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V	
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V	
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V	
V <sub>RST</sub>	Power-up output low voltage <sup>3</sup>	V <sub>CC</sub> = 5.5V; I <sub>OL</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND		±0.01	±1		±1	µA	
I <sub>I</sub>	Input leakage current 74ABTH16823A	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	±0.01	±1		±1	µA	
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub>	Data pins	0.01	1		1	µA	
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0		-2	-3		-5	µA	
I <sub>HOLD</sub>	Bus Hold current inputs <sup>5</sup> 74ABTH16823A	V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0.8V	35			35		µA	
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 2.0V	-75			-75			
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0 to 5.5V	±800						
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	µA	
I <sub>PU/PD</sub>	Power-up/down 3-State output current <sup>4</sup>	V <sub>CC</sub> = 2.1V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = GND or V <sub>CC</sub> , V <sub>OE</sub> = Don't care		±5.0	±50		±50	µA	
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		1.0	10		10	µA	
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-1.0	-10		-10	µA	
I <sub>CEX</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		50	50		50	µA	
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-50	-80	-180	-50	-180	mA	
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	1		1	mA	
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		9.0	19		19	mA	
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	1		1	mA	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		0.2	1		1	mA	

### NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V with a transition time of up to 10msec. From V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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74ABTH16823A

## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT	
			$T_{amb} = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$			$T_{amb} = -40^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$			
			MIN	TYP	MAX	MIN	MAX		
$f_{MAX}$	Maximum clock frequency	1	140	190		140		MHz	
$t_{PLH}$ $t_{PHL}$	Propagation delay nCP to nQx	1	1.4 1.2	2.3 1.9	3.2 2.6	1.4 1.2	3.7 2.9	ns	
$t_{PHL}$	Propagation delay nMR to nQx	2	2.0	3.3	4.3	2.0	5.0	ns	
$t_{PZH}$ $t_{PZL}$	Output enable time to High and Low level	4 5	1.3 1.2	2.4 2.1	3.2 2.9	1.3 1.2	3.9 3.4	ns	
$t_{PHZ}$ $t_{PLZ}$	Output disable time from High and Low level	4 5	1.7 1.6	2.9 2.3	4.0 3.2	1.7 1.6	4.7 3.4	ns	

## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_{amb} = -40 \text{ to } +85^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low nDx to nCP	3	2.0 1.5	1.3 0.9	2.0 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3	1.5 1.5	-0.9 -1.2	1.5 1.5	ns
$t_w(H)$ $t_w(L)$	nCP pulse width High or Low	1	3.3 3.3	1.7 1.7	3.3 3.3	ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low nCE to nCP	3	1.5 2.0	0.9 0.9	1.5 2.0	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nCE to nCP	3	1.5 1.5	-0.8 -0.9	1.5 1.5	ns
$t_w(L)$	nMR pulse width, Low	2	3.0	1.7	3.0	ns
$t_{rec}$	Recovery time nMR to nCP	2	2.5	1.0	2.5	ns

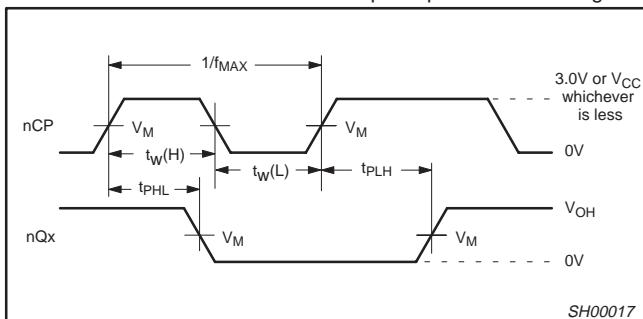
# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

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74ABTH16823A

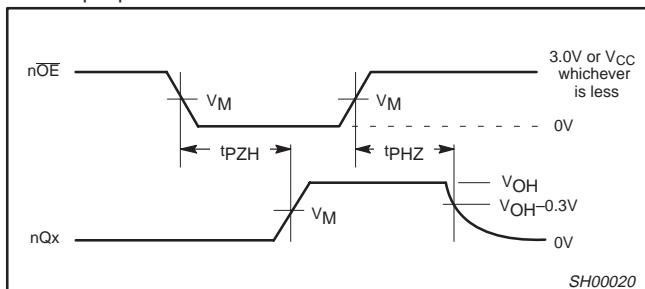
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

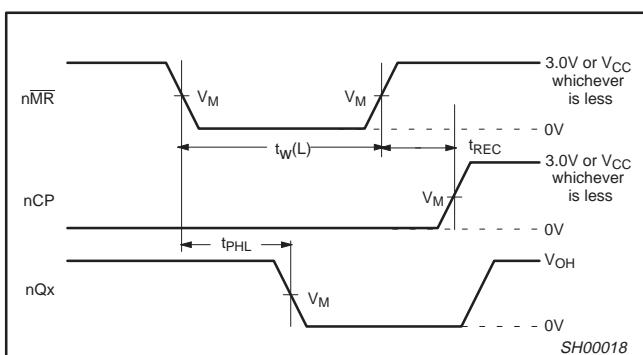
The shaded areas indicate when the input is permitted to change for predictable output performance.



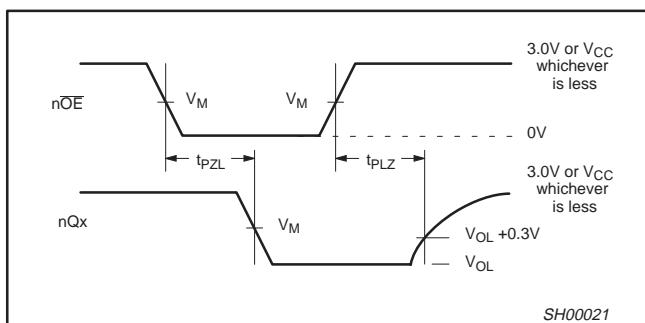
**Waveform 1. Propagation Delay, Clock Input to Output,  
Clock Pulse Width, and Maximum Clock Frequency**



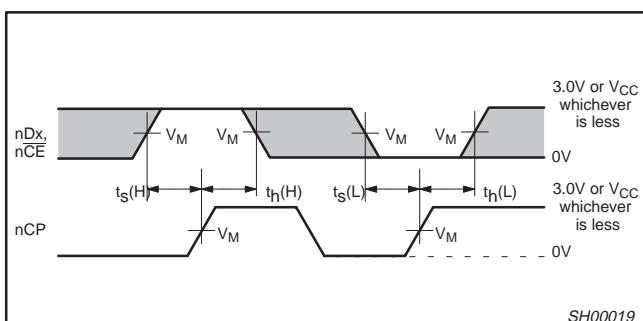
**Waveform 4. 3-State Output Enable Time to High Level  
and Output Disable Time from High Level**



**Waveform 2. Master Reset Pulse Width, Master Reset to  
Output Delay and Master Reset to Clock Recovery Time**



**Waveform 5. 3-State Output Enable Time to Low Level  
and Output Disable Time from Low Level**

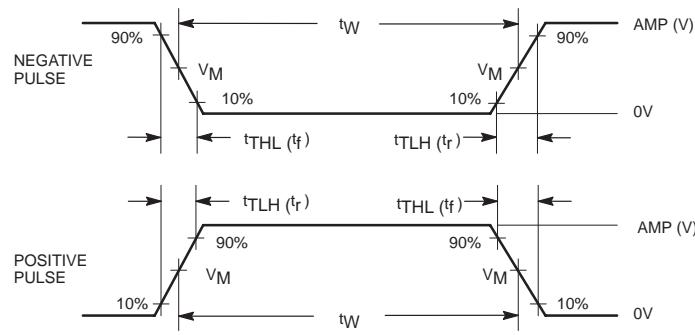
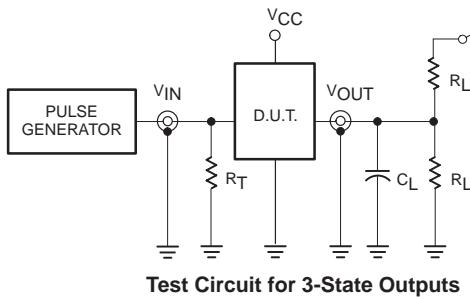


**Waveform 3. Data Setup and Hold Times**

# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823A  
74ABTH16823A

## TEST CIRCUIT AND WAVEFORM



### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS:

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_R$	$t_f$
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

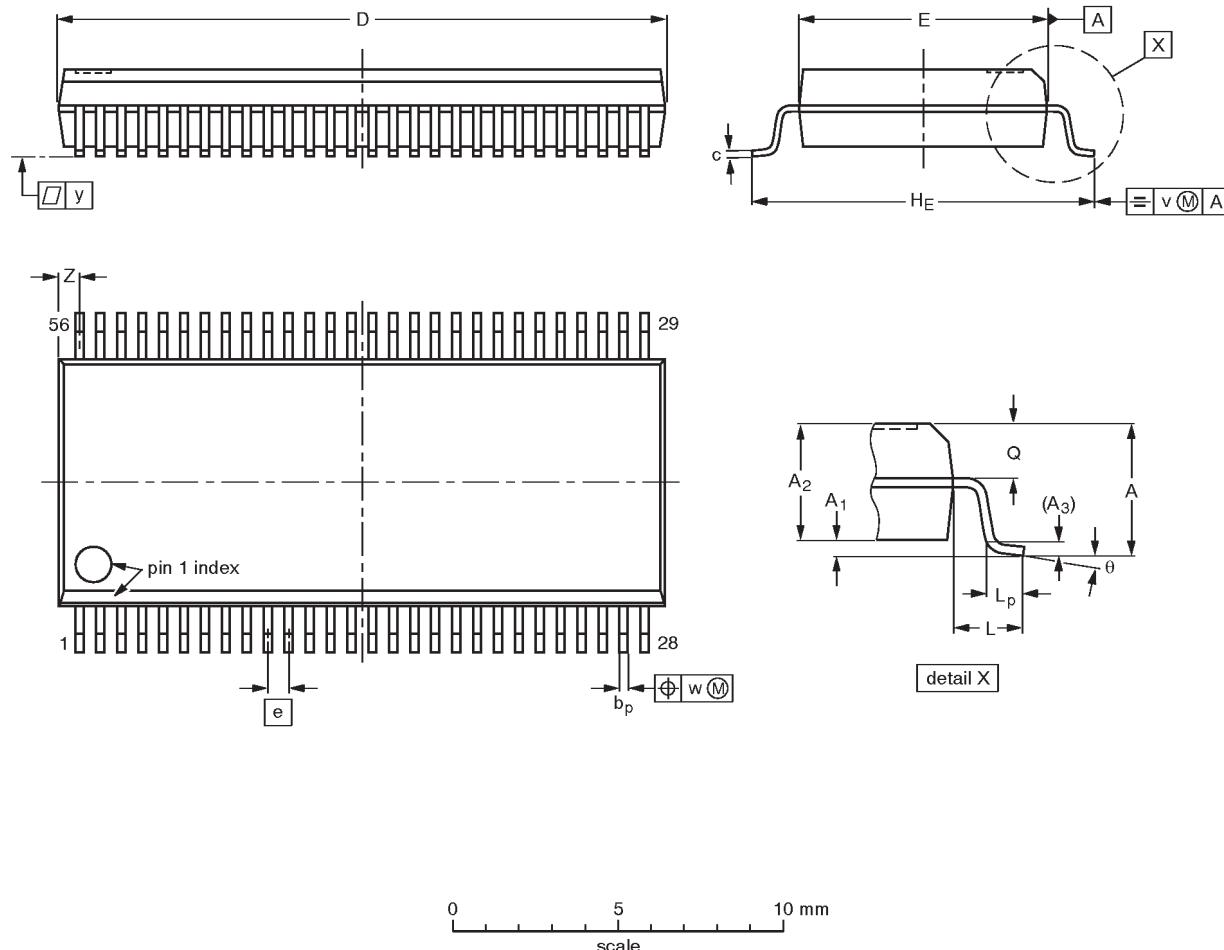
SH00022

**18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)**

**74ABT16823A  
74ABTH16823A**

**SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm**

**SOT371-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	theta
mm	2.8 0.2	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

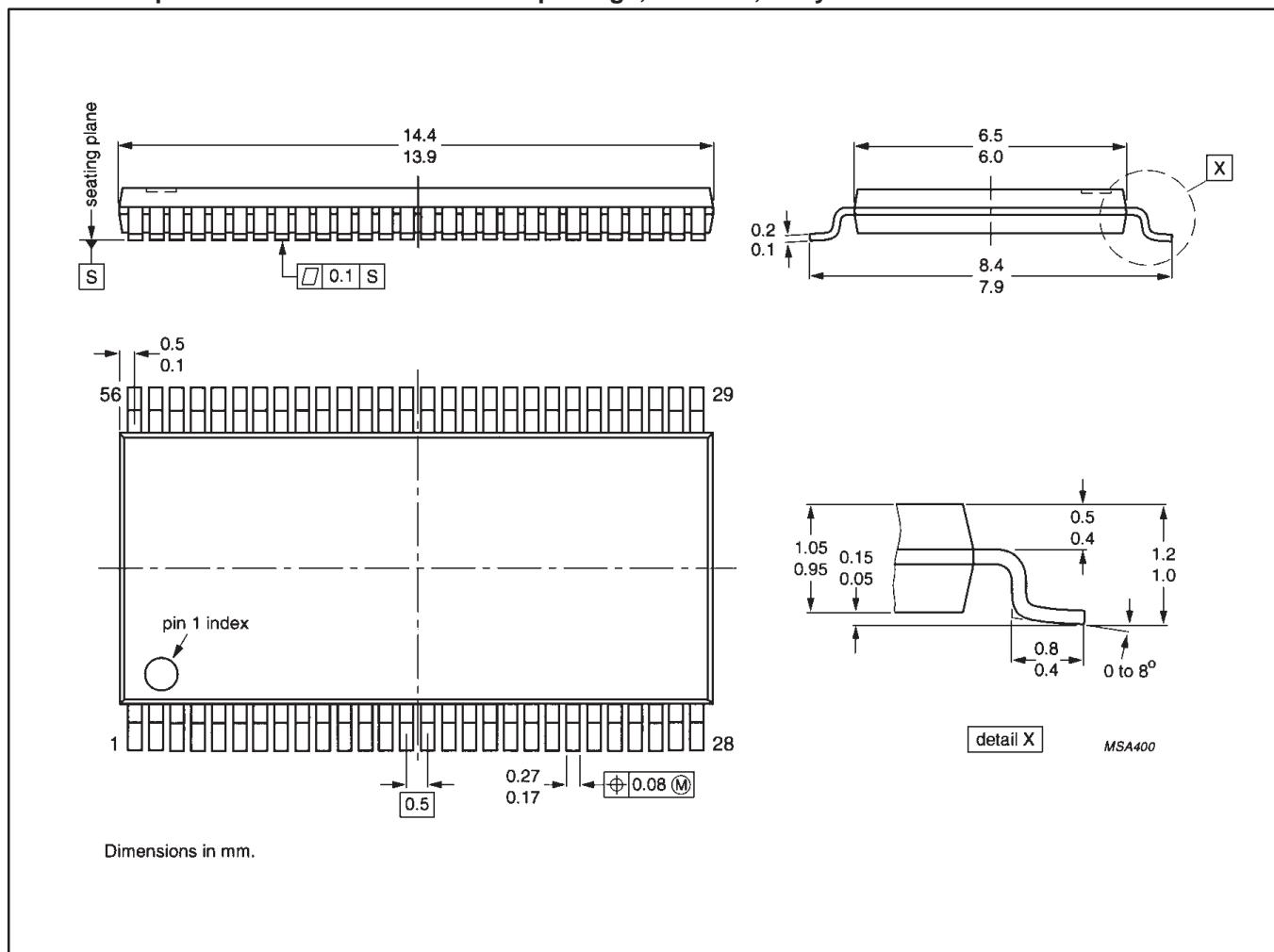
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)

74ABT16823A  
74ABTH16823A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823A  
74ABTH16823A

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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